

09/917,238

L Number	Hits	Search Text	DB	Time stamp
1	2667	phase adj1 alignment	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:18
2	141374	multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:20
3	83	(phase adj1 alignment ) same multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:20
4	17	sampl\$3 same ((phase adj1 alignment ) same multiplexer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 09:37
5	9035	clock near2 recovery	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
6	335	(phase adj1 alignment ) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
7	304761	oscillator	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
8	3708	barrel adj2 shift\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 10:10
9	5	((phase adj1 alignment ) and (clock near2 recovery)) and oscillator and (barrel adj2 shift\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:04
10	2	6414523.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:06
11	2	(phase adj1 alignment ) same (barrel adj2 shift\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:07
12	27	(phase adj1 alignment ) and (barrel adj2 shift\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:16
13	8	(barrel adj2 shift\$3) and ((phase adj1 alignment ) same multiplexer)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:18
14	1		USPAT	2004/10/27 11:18
15	1		USPAT	2004/10/27 11:18
16	968	pulse adj1 width adj1 adjust\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:19
17	1400	pulse adj1 width adj1 adjust\$4	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:19
18	2	(phase adj1 alignment ) and (pulse adj1 width adj1 adjust\$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20

19	131	(pulse adj1 width adj1 adjust\$4) and multiplexer	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
20	1	((pulse adj1 width adj1 adjust\$4) and multiplexer) and (barrel adj2 shift\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
21	1	((pulse adj1 width adj1 adjust\$4) and multiplexer) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:20
22	31	((phase adj1 alignment ) same multiplexer) and (clock near2 recovery)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:29
23	19	(phase adj1 alignment ) and multiplexer and (barrel adj2 shift\$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT	2004/10/27 11:29

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**1 Single-chip 1062 Mbaud CMOS transceiver for serial data communication**

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Kanellos, G.T.; Stampoulidis, L.; Pleros, N.; Houbavlis, T.; Tsiokos, D.; Kehayas, E.;  
 Avramopoulos, H.; Guekos, G.;  
 Photonics Technology Letters, IEEE, Volume: 15, Issue: 11, Nov. 2003  
 Pages:1666 - 1668

[\[Abstract\]](#) [\[PDF Full-Text \(348 KB\)\]](#) IEEE JNL
**3 Architecture and methodology of a SoPC with 3.25Gbps CDR based SERDES and 1Gbps dynamic phase alignment**

Venkata, R.; Wong, W.; Tran, T.; Chan, V.; Hoang, T.; Lui, H.; Ton, B.; Shumurayev, S.;  
 Lee, Shoujun Wang; Huy Ngo; Kabani, M.; Maruri, V.; Tin Lai; Tam Nguyen; Zaliznyak, A  
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[\[Abstract\]](#) [\[PDF Full-Text \(398 KB\)\]](#) IEEE CNF
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Gursoy, Z.O.; Leblebici, Y.;  
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**7 A 20-Gb/s CMOS multichannel transmitter and receiver chip set for ultra-high-resolution digital displays**  
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**9 SONET requirements for jitter interworking with existing networks**  
*Nunn, R.O.;*  
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